**ECE 121DA Semiconductor Processing and Device Design**

**Winter 2023 Design Project Phase #1**

**(Report Deadline: Friday March 17, 2023, Midnight)**

This design project is divided into two phases. The first and second phases will take about 3.5 weeks each. You should work as a team of 4-5 engineers with some responsible for the *n*-channel MOSFET and the others responsible for the *p*-channel MOSFET design. The engineers must divide the work among them and ***integrate*** the separate parts into a cohesive overall project. The design project presentations and reports should **clearly highlight the individual contributions**. A short report and an interview (15 min/group) are due after Phase #1. [A final report and an in-class presentation (20 min/group) combining the content of Phase #1 and #2 are due at the end of next quarter].



1. Design a Si *n*-channel/*p*-channel MOSFET with a printed gate length of 1.8 m and silicon dioxide gate dielectric thickness of 25 nm. The various doping requirements are specified in the following table.

|  |  |  |
| --- | --- | --- |
|  | ***N*-channel MOSFET** | ***P*-channel MOSFET** |
| **Polysilicon** | Uniform doping with P of 1020 cm-3. | Uniform doping with B of 1020 cm-3. |
| **Substrate\*** | Uniform doping with B of 3×1015 cm-3. | Uniform doping with P of 3×1015 cm-3. |
| **Source/Drain** | Gaussian doping with As. The peak doping concentration is at the surface with 2×1020 cm-3, lateral factor is 0.75 by using error function, and junction depth is 0.3 m. | Gaussian doping with B. The peak doping concentration is at the surface with 2×1020 cm-3, lateral factor is 0.75 by using error function, and junction depth is 0.3 m. |
| **Channel** | Gaussian doping with B. The peak doping concentration is at the surface with 3×1016 cm-3 and ‘junction’ depth is 0.22 m. | Gaussian doping with P. The peak doping concentration is at the surface with 3×1016 cm-3 and ‘junction’ depth is 0.22 m. |

\* There can be only one substrate… pick one!

* 1. Simulate the *ID-VG* characteristics at low *VD* = +0.1 V for NMOS (and -0.1 V for PMOS) and high *VD* = +1.5 V for NMOS (and -1.5 V for PMOS). Use a *VG* range of -0.5 to +1.5 V for NMOS (and +0.5 to -1.5 V for PMOS).
  2. Extract the device threshold voltage (*Vth*) from the *ID-VG* characteristics at low *VD*. Compare the simulation result with the theoretical value.
  3. Extract the subthreshold swing from the *ID-VG* characteristics at low *VD*.
  4. Compare the difference in the corresponding *VG* at *ID* = +0.1 A/m for NMOS (and -0.1 A/m for PMOS) from the low and high *VD*.
  5. Compute the maximum transconductance (*gm*) from the *ID-VG* characteristics atlow *VD*. Compare the simulation result with the theoretical value.
  6. Simulate the *ID-VD* characteristics at gate overdrive (*VG – Vth*) of 0 to +1 V with +0.2 V increment for NMOS (and 0 to -1 V with -0.2 V increment for PMOS). Use a *VD* range of 0 to +1.5 V for NMOS (and 0 to -1.5 V for PMOS).
  7. Simulate the change in *Vth* at substrate bias (*VB*) of 0 to -6 V with -2 V increment for NMOS (and 0 to +6 V with +2 V increment for PMOS).

1. In order to shift the MOSFET *Vth­­*, one can change either the channel doping concentration or the gate electrode work function.
   1. For the *n*-channel MOSFET, replace the *n+* polysilicon gate electrode with *p*+ polysilicon. For the *p*-channel MOSFET, replace the *p+* polysilicon gate electrode with *n+* polysilicon. Extract the new device *Vth* and discuss.
   2. Design a new channel doping recipe to lower the device *Vth* that brings the off-state current to +1 nA/m for NMOS (-1 nA/m for PMOS) for high performance device application. Simulate the *ID-V*G characteristics at high *VD* and plot the results in log scale.
2. Scale the printed gate length from 1.8 to 0.5 m without changing any other parameters and dimensions. Perform 1 b), c), and d) and plot these parameters at printed gate length of 1.8 m, 1.5 m, 1.0 m, and 0.5 m.

\* As a group of four or five, you should hand in your report and presentation in electronic copy. In addition, submit your simulation input files through the course website before the due date.

***\*\*\* Guidelines on Phase 1 Report and Presentation grading \*\*\****

1. Report (33% of the course grade):
   1. (75%) Simulation (e.g. completeness, correctness, etc.)
   2. (10%) Comparison with theoretical values
   3. (15%) Explanation of results

\* Bonus will be given to well-integrated reports and outstanding approaches.